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Transparent Active Matrix Organic Light-Emitting Diode Displays Driven by Nanowire Transistor Circuitry

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ABSTRACT

Optically transparent, mechanically flexible displays are attractive for next-generation visual technologies and portable electronics. In principle, organic light-emitting diodes (OLEDs) satisfy key requirements for this application—transparency, lightweight, flexibility, and low-temperature fabrication. However, to realize transparent, flexible active-matrix OLED (AMOLED) displays requires suitable thin-film transistor (TFT) drive electronics. Nanowire transistors (NWTs) are ideal candidates for this role due to their outstanding electrical characteristics, potential for compact size, fast switching, low-temperature fabrication, and transparency. Here we report the first demonstration of AMOLED displays driven exclusively by NW electronics and show that such displays can be optically transparent. The displays use pixel dimensions suitable for hand-held applications, exhibit 300 cd/m^2 brightness, and are fabricated at temperatures suitable for integration on plastic substrates.

For future display technologies, there is significant interest in extending flat panel approaches to provide optical transparency and/or mechanical flexibility along with direct optical emission (instead of backlighting). Current-generation organic light-emitting diodes (OLEDs) can provide both the required performance and the transparency/flexibility. After the first demonstration by Tang et al. of small-molecule devices,[1] OLEDs using fluorescent or phosphorescent emissive materials have steadily advanced in performance for flat panel display applications.[2–4] Among current-generation electroluminescent materials, both small molecules and polymers are promising for full-color active matrix OLED (AMOLED) displays due to their high external quantum efficiencies, long lifetimes, excellent color purity, and low power consumption.[5] In this regard, solution processing of semiconducting polymers enables both spin-coating and printing methods for large-area-display fabrication.

The realization of displays which are transparent and/or flexible will also require the challenging realization of transparent transistor and circuit integration strategies. Importantly, the circuitry required for each AM display pixel must contain at least one switching transistor, one driver transistor, and a storage capacitor, with appropriate scan and data lines to allow selective pixel addressing. The drive transistors must provide sufficient current for the OLED pixels, higher than that required for liquid-crystal display (LCD) elements, in the 1–5 μA/pixel range for high-resolution displays. Thin-film transistors (TFTs) using low-temperature polysilicon (LTPS) or amorphous silicon (α-Si) channels can provide such drive currents when fabricated on glass substrates using opaque contacts; indeed, AMOLED displays incorporating LTPS or α-Si TFTs have been demonstrated.[4,6–8] However, conventional poly Si TFT and α-Si TFT backplanes are optically opaque and not well-suited for flexible displays requiring low-temperature processing (e.g., on polymers). While organic thin-film transistors (OTFTs) are compatible with low-temperature processing and some are optically transparent,[9,10] they have relatively low carrier mobilities and typically utilize relatively long channel lengths, dictating relatively large transistor areas to provide the required drive current. Architectures in which the TFT area becomes comparable to that of the pixel emitter area significantly restrict the aperture ratio, leading to unacceptable brightness resolution—power consumption

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trade-offs. Low-mobility channels also may restrict drive circuitry operating frequencies, limiting the display response time.

Nanowire transistors (NWTs), transistors having one or more semiconductor nanowires as the active channel region, potentially offer the performance required for AMOLED circuitry along with desired transparency and processing characteristics. Indeed, recent reports indicate significantly greater NWT response characteristics versus LTPS/α-Si TFTs in terms of current per unit width and carrier mobility.[11–14] Approaches in which NWs are synthesized on sacrificial substrates and then straightforwardly transferred to the device substrate allow realization of high-performance channel regions without high-temperature processing. NWTs have also been shown to perform well in flexible electronics applications,[15–17] and fully transparent NWTs on glass and plastic substrates using wide-band gap NWs with transparent gate and source–drain (S–D) electrodes have recently been demonstrated.[18,33]

Here we report the first transparent AMOLED display elements in which the switching and driving circuits are comprised exclusively of NWT electronics fabricated at room temperature via a simple and scalable process. We use In_2O_3 nanowires as active channel materials, a performance-enhancing high-*k* organic self-assembled nanodielectric (SAND) as the gate insulator, and indium tin oxide (ITO) as the transparent conducting gate and S–D electrodes. Proof-of-concept green-emitting polymer LEDs (PLEDs) utilizing high-efficiency interfacial charge-blocking and EL materials are integrated with a transparent bottom contact electrode for efficient optical emission through the glass substrate and an opaque or semitransparent top contact (cathode), allowing emission through both the top and bottom sides of the structure. Here, NWTs serve as control and drive circuitry elements for 54 × 176 μm OLED pixels, with the circuit for a unit pixel consisting of one switching NWT, two parallel driving NWTs, and one storage capacitor. The active pixel elements are organized into rectangular arrays covering areas up to 2 × 2 mm and containing up to 300 pixels and 900 NWTs per array. Each pixel within an array is controlled by scan lines, data lines, V_{dd} lines, and a common cathode line. We also show that, using appropriate gate and interconnect dielectrics, NW-AMOLED displays can be fabricated in a low-complexity process, requiring only 4 photomasks versus ~8–10 photomasks for a typical poly-Si TFT AMOLED display.

The fabrication begins with a 200 nm thick SiO_2 layer deposited by e-beam evaporation on Corning 1737A glass substrates as a buffer layer for planarization. Next, a 100 nm ITO thin film is deposited by ion-assisted deposition (IAD) at room temperature (R_{sheet} = 60 Ω/□) and subsequently patterned by photolithography for individually addressed bottom gate electrodes. Next, a 22 nm layer of SAND is deposited on the patterned ITO gate electrodes via solution self-assembly.[31] Following SAND deposition, contact holes are patterned as anode openings for OLED units and as bottom gate electrode contacts for the pixel. Next, a suspension of single-crystal In_2O_3 nanowires, synthesized by pulsed laser ablation,[32] in VLSI-grade 2-propanol is dispersed on the device substrates. The NWs have an average diameter and length of 50 nm and 5 μm, respectively. ITO S–D electrodes are then deposited by IAD at room temperature and patterned by lift-off. Ultrasonication is used to remove NWs outside of the device regions, leaving the NWs which are addressed between the S–D electrodes. Following S–D electrode patterning, the NWTs are subjected to UV ozone cleaning for 1 min to achieve optimum transistor I_{on}, I_{on}/I_{off}, SS, and μ.[23] Next, a 200 nm thick SiO_2 layer is deposited by e-beam evaporation to passivate the device and planarize the NWT array for PLED fabrication. Via holes are next opened to expose the PLED ITO anodes, and PEDOT-PSS (Baytron P) is spin-coated onto the NWT arrays at 2500 rpm for 1 min, followed by drying at 120 °C for 8 min. Next, the TPD–Si_2 + TFB polymer blend HTL + EBL is spin-coated onto the PEDOT-PSS-coated ITO film to form a double-layer HTL. Then, a well-balanced charge transport/emissive layer (EML), a TFB + F8BT blend (TFB/F8BT = 1:4), is spin-coated onto the HTL-coated substrates from xylene solution, resulting in a ~70 nm EML. Inside of a glovebox, LiF and Al are thermally evaporated onto the EML at $<10^{-6}$ Torr using a shadow mask to define electrode areas. The NW-AMOLED devices are then encapsulated with glass using an UV-curable epoxy. An electrical measurement jig is used to make electrical connections required to drive the NW-AMOLED displays.

Top and cross-sectional views of the present NWT structure and a pixel electrode for a single pixel are shown in Figure 1a. For ease of viewing, the OLED layers are omitted. A bottom gate transistor structure (ITO S–D electrodes/In_2O_3 NW/SAND/bottom ITO gate electrodes) is employed here. The SAND gate insulator (thickness ~22 nm, leakage current ~30 pA at 2 V) provides a high breakdown voltage and low interface trap density, with a high μ, a steep SS, low operating voltage, and high I_{on}/I_{off}.[14,20–22] A field emission scanning electron microscope (FE-SEM) image of several 54 × 176 μm pixels within a 2 × 2 mm array (30 × 10 pixels) is shown in Figure 1b. The equivalent circuit for a single active pixel, shown in Figure 1c, consists of one switching transistor (T1), two driving transistors (T2 and T3), and one storage capacitor (C_{st}). T1 is employed to select a specified pixel and transfer data through the data line to the OLED. For time-varying operation, data are stored in C_{st} during one period. The current supplied to the OLED is adjusted by controlling the V_{gs} of T2 and T3, equal to the voltage difference of the ends of C_{st}. The EL opening area on the unit pixel is 20 × 106 μm, corresponding to an aperture ratio of ~46%. However, the aperture ratio for the light-emitting areas at a given pixel spacing could, in principle, be as high as 90% using an optimized layout. Since NWTs containing only a few NWs can provide a sufficient drive current for a pixel, the area of the transistor circuitry can be significantly reduced as techniques to place and align nanowires advance. Furthermore, the transparent NWTs should allow stacking of the EL elements and circuit regions with only a modest increase in process complexity. The improved aperture ratio would

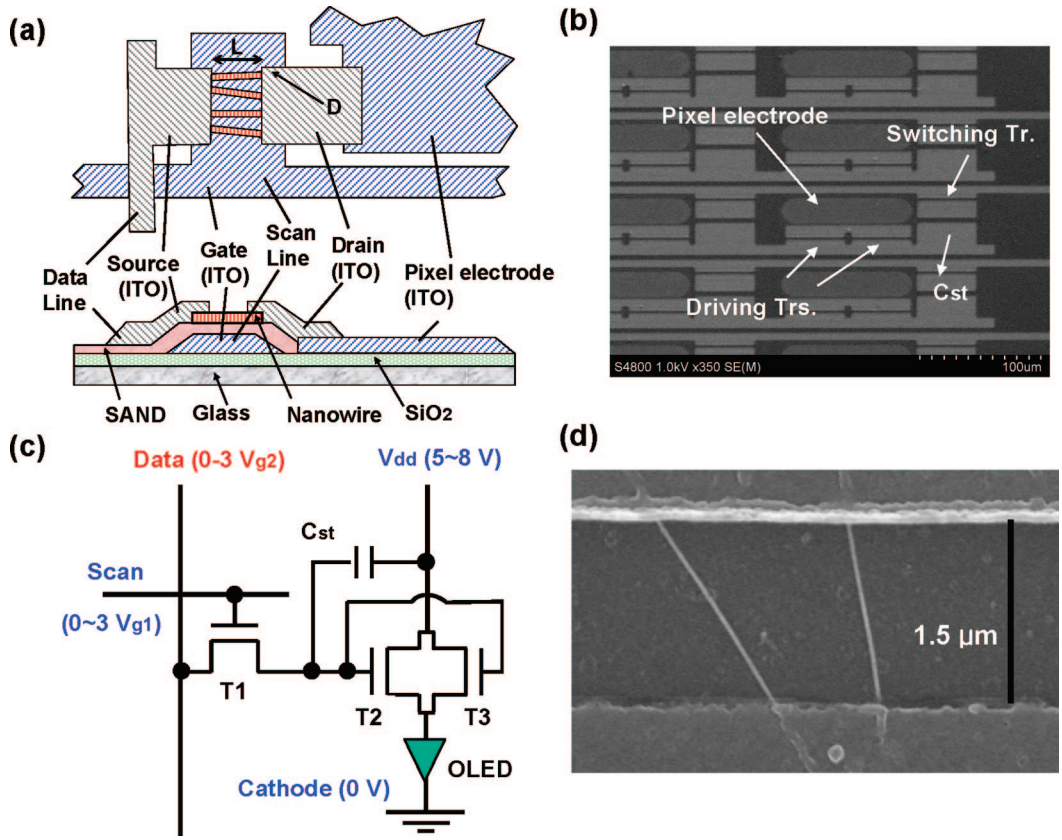

Figure 1. Structure of the drive transistor in a NW-AMOLED array. (a) Top and cross-sectional views of the NWT structure consisting of a SiO_2 buffer layer (200 nm), patterned ITO gate electrode (100 nm), SAND gate dielectric (24 nm), multiple In_2O_3 nanowires for the active channel, ITO for the S–D electrodes (100 nm), and a SiO_2 passivation layer (200 nm). The ITO pad on the right serves as the OLED cathode. (b) Top-view FE-SEM image of several 54 × 176 μm pixels within a 2 × 2 mm NWT array layout, showing OLED cathodes (rectangles with rounded ends), along with control transistors. (c) Schematic for the circuit of a single pixel, consisting of one switching transistor (T1), two driving transistors (T2 and T3) and one storage capacitor. The bias conditions to operate the transistor circuit are 3 V on the scan line for full turn-on, varying 0 to 3 V on the data line, 5–8 V on the V_{dd} line, and 0 V on the cathode line. (d) FE-SEM image of a representative region within a NWT transistor channel, showing multiple In_2O_3 NWs connected between S–D electrodes. The diameter of a NW and the channel length between S–D electrodes of the device are ~50 nm and ~1.5 μm, respectively. Scale bar = 1.5 μm.

therefore provide higher display brightnesses at lower current densities, resulting in improved device lifetimes. Figure 1d shows a FE-SEM image of representative In_2O_3 NWs connected between the transistor S–D electrodes. Note that to maximize transistor performance, the ITO gate overlaps with the ITO S–D electrodes to ensure gating of the full length of the NW channel. Transistor regions on the pixels were imaged by FE-SEM, and the number of In_2O_3 NWs connected between S and D electrodes on the switching and driving transistors of each pixel was 4–8. The In_2O_3 NW diameters and the channel lengths between S–D electrodes along each NW axis are 40–50 nm and 1.2–1.6 μm, respectively.

Figure 2 shows the measured current–voltage (I–V) characteristics of representative NWTs and pixel driver circuits fabricated adjacent to the 2 × 2 mm pixel array but not connected to OLEDs. The design of these patterns, including width and length, are the same as those of the NWT circuits in the pixel array, except for adding extended contact pads for electrical probing. To optimize TFT performance, the following surface treatments were performed: (i) Following NW deposition, plasma etching was performed for 90 s in Ar and O_2 on only the S–D contact region of NWs (the NW active regions were covered with photoresist); (ii) after ITO deposition, the active NWT regions were subjected to ozone treatment for 1 min to remove defects and contaminants on the NW surface and to adjust the relative work functions of the In_2O_3 NWs and the ITO S–D material.[23] On the basis of the ITO work function (Φ_{ITO} = 4.9 eV), it is expected that the ITO S–D contacts will form a relatively low charge injection barrier height to n-type In_2O_3. The transistor performance characteristics in terms of I_{on}/I_{off}, SS, and V_T improve significantly after these treatments. Figure 2a shows a family of drain current versus gate–source voltage (I_{ds}–V_{gs}) plots for a representative NWT. The In_2O_3 NWTs exhibit an I_{on} of ~1 μA (at V_{gs} = 3.0 V, V_{ds} = 0.1 V), $I_{on}/I_{off} = 10^5$, V_T = 0.1 V, SS = 0.25 V/dec, and μ ~258 $cm^2\ V^{-1}\ s^{-1}$. A combination of the cylinder-on-plate capacitance model and the metal-oxide semiconductor FET model was used to extract mobilities.[24] The mobilities of the present SAND-based In_2O_3 NWTs are comparable to or greater than those recently reported for In_2O_3 NWs on oxide dielectrics (μ ~ 6.9–279.1 $cm^2\ V^{-1}\ s^{-1}$) and bulk single-crystal In_2O_3 (μ ~ 160 $cm^2\ V^{-1}\ s^{-1}$).[25–28] It is expected that the single-crystal nature of the In_2O_3 NWs will afford high mobility by decreasing scattering at intergrain regions. In

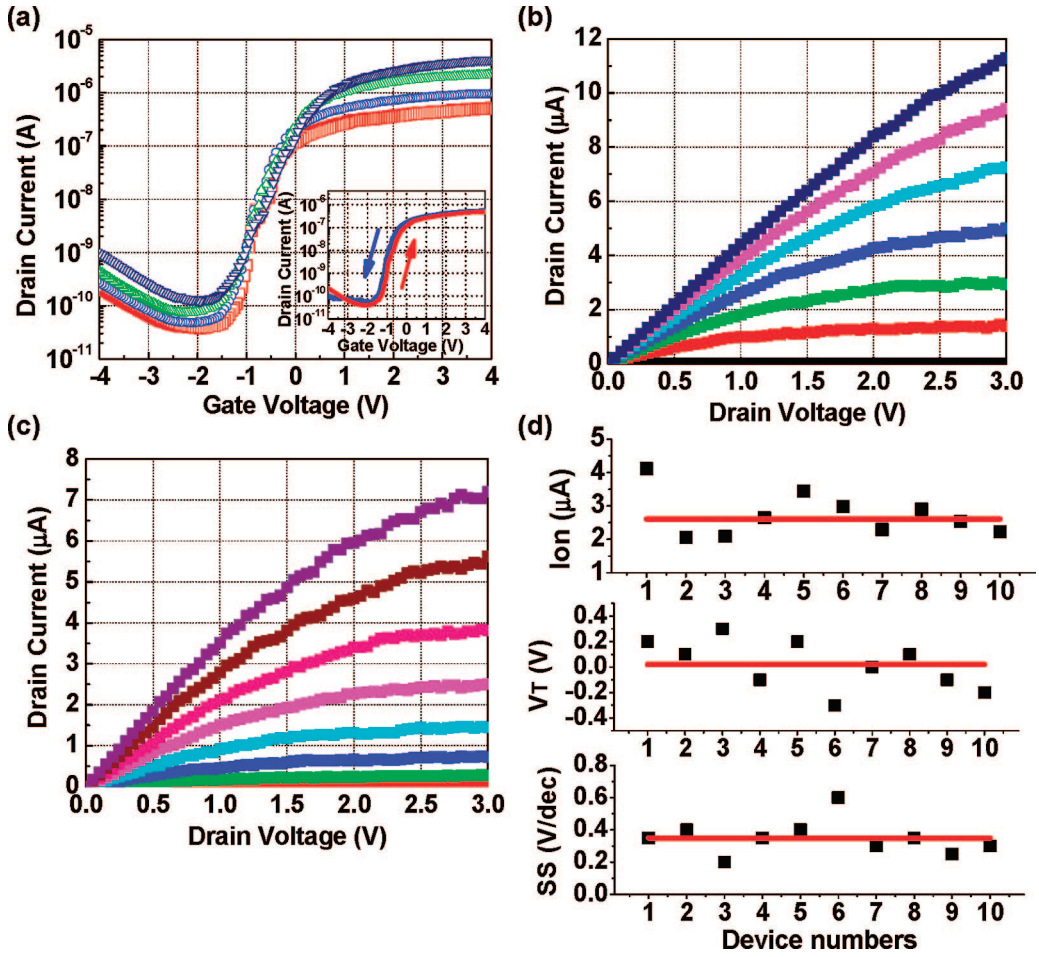

Figure 2. Measured characteristics of fully transparent In_2O_3 NWTs and a single-pixel drive circuit. (a) I_{ds}–V_{gs} characteristics (log scale) of a representative In_2O_3 NWT ($D/L \sim 50$ nm/1.5 μm) with red, blue, green, and dark blue data points corresponding to $V_{ds} = 0.1$, 0.2, 0.5, and 1.0 V, respectively. The inset shows the device hysteresis at $V_{ds} = 0.1$ V. (b) I_{ds}–V_{ds} characteristics for a representative device, with V_{gs} varying from 0.0 to 3.0 V in 0.5 V steps. (c) Output current–voltage characteristics for a single-pixel circuit consisting of one switching transistor and two driving transistors (I_{ds} versus V_{ds} for the parallel combination of T2 and T3 for various steps in the "data" line voltage (2 V on the scan line to fully turn-on T1, 0.0 to 4.0 V on the data line in 0.5 V steps). (d) The I_{on}, V_T, and SS values of 10 representative devices, with red lines indicating the average values for the respective parameters.

addition, the SAND dielectric is known to enable high performance NWTs with other semiconducting oxides.[14,21–23] The inset in Figure 2a shows device hysteresis for bias sweeps from negative (V_g(–)) to positive gate voltages (V_g(+)) and from V_g(+) to V_g(–). Hysteresis is modest over this bias range, illustrating the excellent quality of the SAND/In_2O_3 NW materials combination and indicating negligible charge trapping and detrapping in/on the SAND and at the NW/SAND interface. The I_{on}, V_T, and SS characteristics of 10 representative transistors are shown in Figure 2d, with red lines indicating average values. I_{on}, V_T, and SS average values are 2.73 μA and 0.02 and 0.35 V/dec, respectively. Note that these parameters were extracted from the I_{ds}–V_{gs} plots at 0.1 V_{ds}. The drain current versus drain–source voltage (I_{ds}–V_{ds}) characteristics of a representative In_2O_3 NWT are shown in Figure 2b, exhibiting typical n-type transistor characteristics. The In_2O_3 transistors exhibit a high $I_{on} \sim 6$ μA at $V_{ds} = 2.0$ V and $V_{gs} = 2.0$ V.

The characteristics of the 3-transistor circuit used to drive a single pixel were also characterized using the circuit topology shown in Figure 1c but omitting the OLED. To operate the transistor circuit, 3.0 V was applied to the scan line to fully turn on the gate of switching transistor T1. Figure 2c shows the measured output current of the circuit (I_{ds} of T2 and T3 in parallel) versus the output voltage V_{dd}. The various curves correspond to various values of the data line voltage (drain of T1: 0.0 to 4.0 V in 0.5 V steps). The steps in the data line voltage correspond to changes in V_{gs} for the drive transistors (T2 and T3). The transistor circuit exhibits $\sim$5 μA at $V_{dd} = 3.0$ V, $V_{g1} = 3.0$ V, and $V_{g2} = 3.0$ V, with the calculated total capacitance of a unit pixel of $\sim$1.3 pF. Of the 70 transistor circuits measured, more than 60 circuits operated properly. Thus, in the present laboratory-scale experiments, the NWT circuit yields are $\sim$90%. The sizable μ and steep SS parameters of the SAND-based In_2O_3 NWTs should enable smaller transistor areas and fulfill AMOLED transistor requirements for rapid switching and high speeds. Sufficiently rapid switching should enable direct digital pixel driving, which would reduce the interface circuitry complexity.

The present NW-AMOLED devices consist principally of two parts, transistor circuits and OLEDs. For transistor

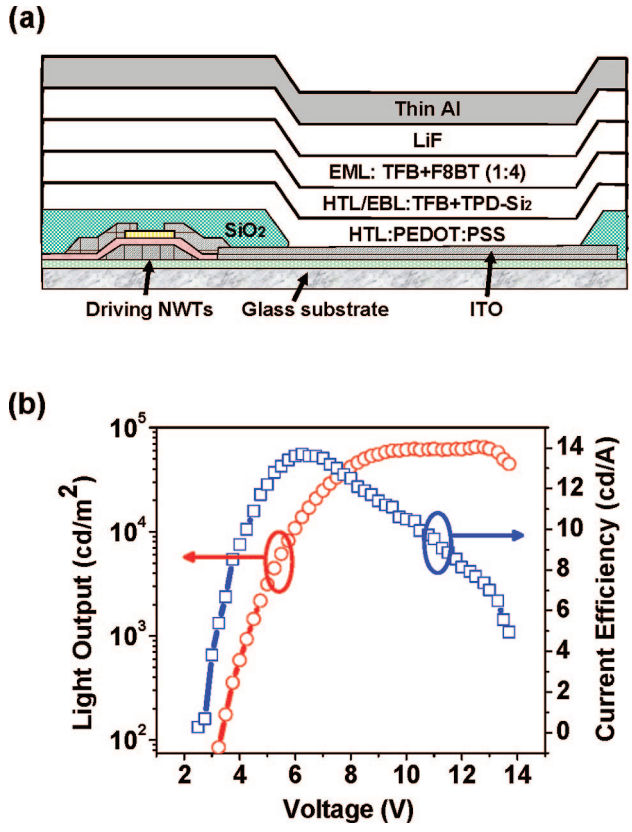

Figure 3. OLED device structure and measured parameters. (a) Cross-sectional view of the EL structure employing an ITO anode and an Al cathode. (b) Luminescence and current efficiency versus voltage characteristics of the polymer OLED structure measured in a large-area device.

circuits, key factors are NWT performance, uniform NW assembly on large substrates, a high-quality gate insulator, and effective passivation. Implementation of an appropriate OLED structure is also important. The cross-section of the device structure used in the present NW-AMOLED devices is shown in Figure 3a. The multilayer PLED structure consists of (i) an ITO anode, (ii) a PEDOT-PSS (poly(3,4-ethylenedioxythiophene)poly(styrenesulfonate)) hole-injection layer (HIL), (iii) a TFB (poly(9,9-dioctylfluorene-*co*-*N*-(4-(3-methylpropyl)phenyl)diphenylamine)) + $TPDSi_2$ (4,4′-bis[(*p*-trichlorosilylpropylphenyl)phenylamino]biphenyl) hole-transport/electron-blocking layer (HTL/EBL), (iv) a TFB + F8BT (poly(9,9-dioctylfluorene-*co*-benzothiadiazole)) emissive layer (EML), and (v) a LiF/Al electron-injection layer/cathode.[5] Here, PEDOT-PSS and TFB + $TPDSi_2$ function as a double-layer hole-injection/-transport layer as well as an efficient electron-blocking layer.[5] PEDOT-PSS planarizes the ITO film while acting as a hole-transport and buffer layer, decreasing the hole-injection barrier from ITO (the PEDOT-PSS work function straddles that of ITO and TFB + TPD–Si_2) and minimizing device leakage currents. TFB + F8BT is a charge-balanced high-efficiency emissive polymer blend. The thickness of each layer was optimized in control experiments. The luminance and current efficiency versus the bias response for a representative large-area PLED are shown in Figure 3b. This green device has a peak current efficiency of 13 cd/A, peak brightness of over 35,000 cd/m^2, and CIE coordinates of $x = 0.28$ and $y = 0.62$. The AMOLED arrays developed here utilized 54 × 176 μm pixels, providing a resolution comparable to that of a quarter

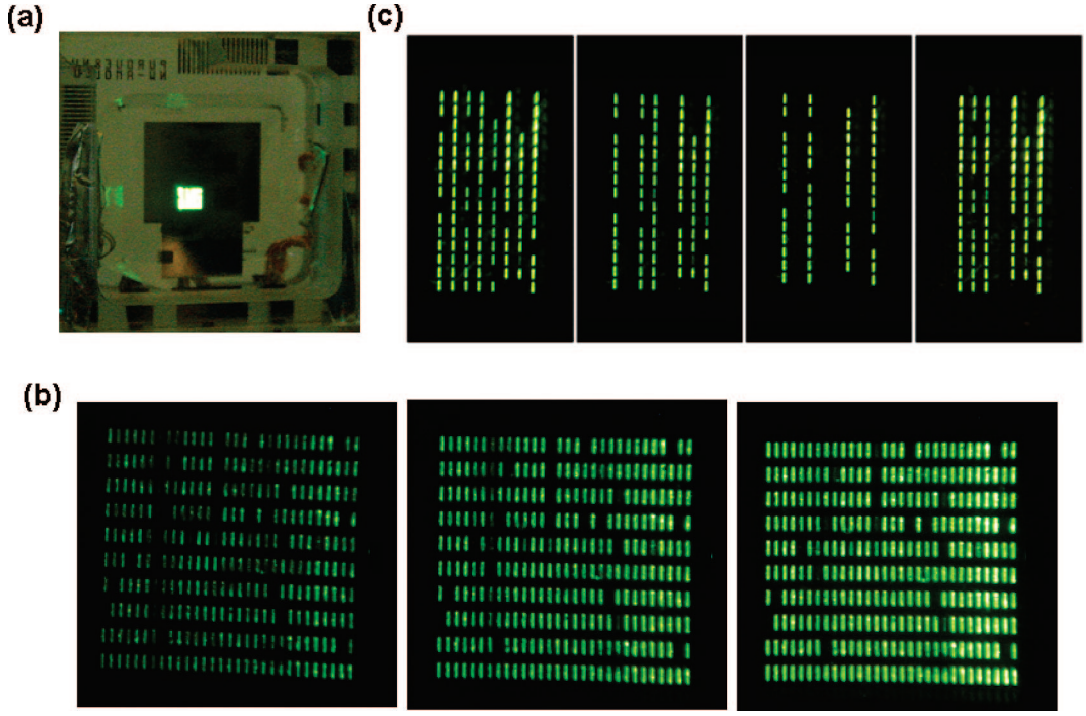

Figure 4. NW-AMOLED display devices. (a) Optical image of a NW-AMOLED substrate consisting of three 2 × 2 mm transistor arrays, plus unit pixels and test devices, showing emission from a 2 × 2 mm AMOLED array. (b) Magnified microscope image of a 2 × 2 mm AMOLED pixel array for various bias conditions (drive circuit: V_{data} are 1, 2, and 3 V with fixed $V_{scan} = 3$ V and $V_{dd} = 5$ V). (c) Optical images of a 15 pixel × 8 pixel array, with selective pixel lines addressed independently by controlling V_{data} lines. In the first image, all data lines are enabled, while various subsets of data lines are turned off in the other images.

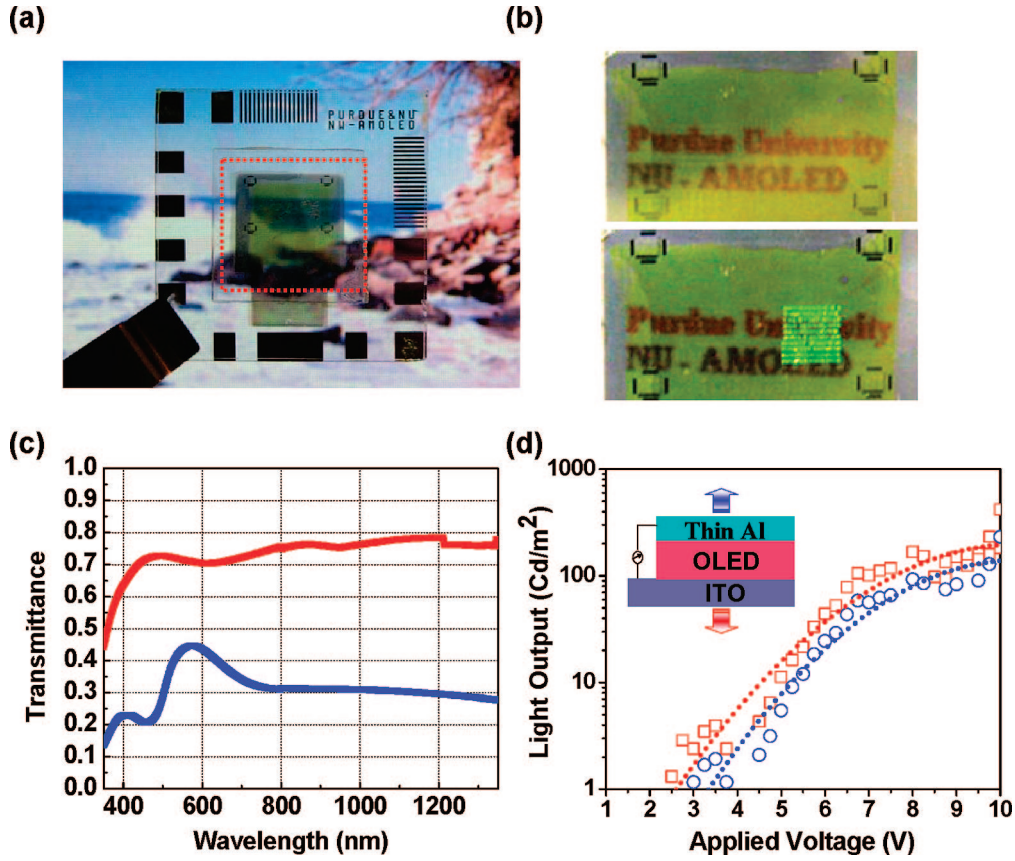

Figure 5. Fully transparent NW-AMOLED display elements. (a) Optical image of a fully transparent NW-AMOLED substrate consisting of three 2 × 2 mm AMOLED pixel arrays, 340 unit pixels, 80 transistor/circuit test devices, 6 alignment marks, 20 test patterns, and contact pads. The feature on the photograph behind the substrate is clearly visible. (b) Optical images of a region of the substrate containing a 2 × 2 mm array (300 pixels, driven by 900 nanowire transistors), showing the pixel array in (i) the off state and (ii) the on state, with 6 pt text on the paper behind the substrate clearly visible. (c) Optical transmission spectrum of regions of a 2 × 2 mm NW-AMOLED display substrate (red line: TFT circuits before OLED deposition; blue line: after transparent OLED deposition). (d) Measured luminance versus supply voltage curve for a 2 × 2 mm AMOLED array with all scan and data lines enabled (V_{scan} = 3 V, V_{data} = 3 V), showing light emission through the Al cathode (circles) and through the glass substrate (squares). A luminance of 300 cd/m^2 is obtained at ~10 V.

video graphics array (QVGA: resolution of 320 × 240) for a 2.65 in. display. Typical target performance levels for such a display include a peak luminescence of 300 cd/m^2 and green CIE coordinates of (0.28, 0.62) using the measured efficiency of the PLED structure and the AMOLED aperture ratio (46%), with the current per pixel required to achieve 300 cd/m^2 estimated to be ~1 μA. Therefore, the present drive current (~5 μA on V_{dd} = 2.0 V, V_{g1} = 3.0 V, and V_{g2} = 3.0 V) is ample to drive the present 54 × 176 μm pixel array at the required brightness.

In initial AMOLED experiments, a thick Al cathode (150 nm) was employed so that the EL generated in the emissive layer passed through the transparent ITO/glass side and was modulated by the driving NWT OLED current control. Figure 4a shows an optical image of a 1 × 1 in. glass substrate containing three 2 × 2 mm AMOLED arrays, 340 unit pixels, 80 test NWT devices, 6 alignment marks, 20 test patterns, and contact pads. The optical image shows visible emission from a 2 × 2 mm NW-AMOLED array (300 pixels: 900 nanowire transistors). For the 2 × 2 mm array, the scan lines for all pixels are connected together, as are the data lines. Figure 4b shows a magnified image of the array at various values of the data line voltage (V_{data} is for 1, 2, and 3 V with fixed 3 V_{scan} and 5 V_{dd}), corresponding to three brightness levels. On the basis of the measured drive current levels (Figure 2c) and the PLED properties (Figure 3b) and assuming a 0.5 V drop across the drive transistor, at the maximum bias point, the efficiency is estimated to be ~11 cd/A and the luminance ~1630 cd/m^2 within the active pixel area, corresponding to an average luminance of ~300 cd/m^2 for the overall array. The corresponding *I*–*V* characteristics of the PLEDs are dependent upon the aggregate properties of all of the interfaces in the device and of the driving NWTs, which are saturated. The great majority of the pixels turn on uniformly, with a few exhibiting a lower than average EL intensity. This may reflect the relatively small numbers of NWs within these NWT circuits, resulting in diminished supply currents to a small number of devices. The dark spots ("dead" pixels) may be due to EL degradation, incomplete pixel opening, or defects on the ITO electrodes. Figure 4c shows optical images of a 15 pixel × 8 pixel array in which the data line for each column is individually addressable. Various combinations of data lines are addressed in the various optical images, illustrating that selected pixel lines can be successfully turned on and off by controlling

V_{data} lines, clearly demonstrating the pixel electrical addressability of these NW-AMOLED displays.

In order to fabricate transparent displays, additional NW-AMOLED arrays were fabricated using a very thin Al (~15 nm) cathode. Figure 5a shows an optical image of the fully transparent NW-AMOLED substrate, with a background image visible through the display region. Optical images of a 2 × 2 mm NW-AMOLED array (300 pixels: 900 nanowire transistors) in the off state and on state are shown in Figure 5b. The text visible through the display is printed using 6 pt font on white paper, indicating fine pixel size. Figure 5c shows optical transmission spectra through the 2 × 2 mm NW-AMOLED display region before OLED deposition (red line) and after OLED deposition (blue line). Optical transmission values are ~72 and ~35% in the 350–1350 nm wavelength range, respectively, without correction for the transmission coefficient of the glass substrate (~91%). The optical transmission properties of these proof-of-concept devices should be readily increased using more transparent OLED designs.[29,30] Transmission coefficients up to 70% have been reported for OLED structures on plastic substrates,[29] although values in the range of 50% are more typical. Measured luminescence versus V_{dd} voltage characteristics are shown in Figure 5d for a device with a 15 nm thick Al cathode, showing the light output measured through both sides of the structure. A luminescence of 300 cd/m^2 is obtained for light emission through the ITO side at 10 V, corresponding to ~650 cd/m^2 luminescence within the EL opening (assuming all pixels emit uniformly). As expected, the luminescence through the Al side is somewhat lower due to the lower optical transparency of the thin Al cathode.

A major advance demonstrated in this study is the simple but powerful layout structure for fabricating the NW-AMOELD displays. Conventional LTPS TFT array processes require 8–10 photomasks, which substantially increase manufacturing costs. Here, we demonstrate a room-temperature four photomask process for fabricating transparent NW-AMOLED displays. The process involves (i) bottom gate patterning and OLED anode patterning of ITO (Mask I), (ii) hole patterning for the contact of drain electrodes and ITO anodes of OLED units after SAND deposition (Mask II), (iii) ITO S–D electrode patterning after NW assembly (Mask III), and (iv) hole patterning for OLED units after a passivation layer to protect the NWTs (Mask IV). The gate electrodes and OLED anode can be patterned together, and no active channel layer patterning is required since a NW assembly (multiple NWs) is used, directly contributing to reduced required photomasks. Note that this simple structure should also minimize parasitic capacitances due to multiple layers (intercross-sectional regions and data lines) between the gate and S–D electrodes. The current layout utilizes relatively large transistor widths to achieve high transistor yields without employing sophisticated NW alignment techniques. As methods to control NW deposition and alignment improve, device areas should be significantly reduced.

In summary, we have demonstrated 2 × 2 mm transparent AMOLED displays using NWTs as the active channel material, SAND as the gate insulator, and polymer OLEDs. A NWT-based fabrication approach is applied to transparent AMOLEDs for the first time. The optical transmittance of 2 × 2 mm NWT arrays is ~72%, and that of the NW-AMOLED display through a thin Al cathode is ~35%, with green peak luminance of >300 cd/m^2. Transparent NWT arrays and OLED pixels should enhance the maximum aperture ratio dramatically, compared to conventional AMOLEDs. These results indicate that NWT device strategies can be optimized for the requirements of applications such as windshield displays, head-mounted displays, transparent screen monitors, mobile phones, PDAs, and handheld personal computers.

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References

(1) Tang, C. W.; VanSlyke, S. A. *Appl. Phys. Lett.* **1987**, *51*, 913–915.
(2) Adachi, C.; Baldo, M. A.; Thompson, M. E.; Forrest, S. R. *J. Appl. Phys.* **2001**, *90*, 5048–5051.
(3) Rajeswaran, G.; Itoh, M.; Boroson, M.; Barry, S.; Hatwar, T. K.; Kahen, K. B.; Yoneda, K.; Yokoyama, R.; Komiya, N.; Kanno, H.; Takahashi, H. *SID Digest* **2000**, *31*, 974–977.
(4) Ju, S. H.; Yu, S. H.; Kwon, J. H.; Kim, H. D.; Kim, B. H.; Kim, S. C.; Chung, H. K.; Weaver, M. S.; Lu, M. H.; Kwong, R. C.; Hack, M.; Brown, J. J. *SID Digest* **2002**, *37.3*, 1096–1099.
(5) Yan, H.; Lee, P.; Armstrong, N.; Graham, A.; Evmenenko, G.; Dutta, P.; Marks, T. J. *J. Am. Chem. Soc.* **2005**, *127*, 3172–3183.
(6) Ucjikoga, S. *MRS Bull.* **2002**, *27*, 881–886.
(7) Madelung, O., Ed. *Technology and Applications of Amorphous Silicon*; Springer: Berlin, 2000.
(8) Snell, A. J.; Mackenzie, K. D.; Spear, W. E.; LeComber, P. G.; Hughes, A. J. *Appl. Phys. Lett.* **1981**, *24*, 357–362.
(9) Gelinck, G. H.; Edzer, H.; Huitema, A.; Veenendaal, E. V.van; Cantatore, E.; Schrijnemakers, L.van der; Putten, J. B. P. H.; Geuns, T. C. T.; Beenhakkers, M.; Giesbers, J. B.; Hiusman, B.-H.; Meijer, E. J.; Benito, E. M.; Touwslager, F. J.; Marsman, A. W.van; Rens, B. J. E.De; Leeuw, D. M. *Nat. Mater.* **2004**, *3*, 106–110.
(10) Klauk, H.; Halik, M.; Zschieschang, U.; Eder, F.; Rohde, D.; Schmid, G.; Dehm, C. *IEEE Trans. Electron Devices* **2005**, *52*, 618–622.
(11) Xiang, J.; Lu, W.; Hu, Y.; Wu, Y.; Yan, H.; Lieber, C. M. *Nature* **2006**, *441*, 489–493.
(12) Cui, Y.; Zhong, Z.; Wang, D.; Wang, W. U.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 149–152.
(13) Cha, S. N.; Jang, J. E.; Choi, Y.; Ho, G. W.; Kang, D.-J.; Hasko, D. G.; Welland, M. E.; Amaratunga, G. A. J. Proceedings of the 35th European Solid-State Device Research Conference, Grenoble, France; 2005; pp 217–220.
(14) Ju, S.; Lee, K.; Janes, D. B.; Yoon, M.-H.; Facchetti, A.; Marks, T. J. *Nano Lett.* **2005**, *5*, 2281–2286.
(15) McAlpine, M. C.; Friedman, R. S.; Jin, S.; Lin, K.-H.; Wang, W. U.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 1531–1535.
(16) Chen, J.; Konenkamp, R. *Appl. Phys. Lett.* **2003**, *82*, 4782–4784.
(17) McAlpine, M. C.; Friedman, R. S.; Lieber, C. M. *Proc. IEEE* **2005**, *93*, 1357–1363.
(18) Ju, S.; Facchetti, A.; Xuan, Y.; Liu, J.; Ishikawa, F.; Ye, P.; Zhou, C.; Marks, T. J.; Janes, D. B. *Nat. Nanotechnol.* **2007**, *2*, 378–384.
(19) Liu, F.; Bao, M.; Wang, K. L.; Li, C.; Lei, B.; Zhou, C. *Appl. Phys. Lett.* **2005**, *86*, 213101/1–213101/3.
(20) Hur, S.-H.; Yoon, M.-H.; Gaur, A.; Facchetti, A.; Marks, T. J.; Rogers, J. A. *J. Am. Chem. Soc.* **2005**, *127*, 13808–13809.
(21) Ju, S.; Janes, D. B.; Lu, G.; Facchetti, A.; Marks, T. J. *Appl. Phys. Lett.* **2006**, *89*, 193506/1–193506/3.

(22) Wang, L.; Yoon, M.-H.; Lu, G.; Yang, Y.; Facchetti, A.; Marks, T. J. *Nat. Mater.* **2006**, *5*, 893–900.
(23) Ju, S.; Lee, K.; Janes, D. B.; Yoon, M.-H.; Facchetti, A.; Marks, T. J. *Nanotechnology* **2007**, *18*, 155201–155207.
(24) Wang, D.; Wang, Q.; Javey, A.; Tu, R.; Dai, H.; Kim, H.; McIntyre, P. C.; Krishnamohan, T.; Saraswat, K. C. *Appl. Phys. Lett.* **2003**, *83*, 2432–2434.
(25) Lei, B.; Li, C.; Zhang, D.; Tang, T.; Zhou, C. *Appl. Phys. A: Mater. Sci. Process.* **2004**, *79*, 439–442.
(26) Zhang, D.; Li, C.; Han, S.; Liu, X.; Tang, T.; Jin, W.; Zhou, C. *Appl. Phys. Lett.* **2003**, *82*, 112–114.
(27) Nguyen, P.; Ng, H. T.; Yamada, T.; Smith, M. K.; Li, J.; Han, J.; Meyyappan, M. *Nano Lett.* **2004**, *4*, 651–657.
(28) Weiher, R. L. *J. Appl. Phys.* **1962**, *33*, 2834–2840.
(29) Uchida, T.; Kaneta, S.; Ichihara, M.; Ohtsuka, M.; Otomo1, T.; Marx, D. R. *J. Appl. Phys.* **2005**, *44*, L282–L284.
(30) Jones, B. A.; Facchetti, A.; Marks, T. J.; Wasielewski, M. R. *Chem. Mater.* **2007**, *19*, 2703–2705.
(31) Yoon, M.-H.; Facchetti, A.; Marks, T. J. *Proc. Natl. Acad. Sci. U.S.A.* **2005**, *102*, 4678–4682.
(32) Li, C.; Zhang, D.; Han, S.; Liu, X.; Tang, T.; Zhou, C. *Adv. Mater.* **2003**, *15*, 143–145.
(33) HollisterM. A. LeJ. D. XiaoG. LuX. KiehlR. A. *DRC Proceedings*; 2007; pp 113–114.
(34) The sheet resistances of the ITO gate and S–D electrodes were measured on a Bia-Rad HL5500 van der Pauw Hall effect measurement system. The optical transmittance spectra of the devices were recorded with a Varian Cary 500 ultraviolet–visible–near-infrared spectrophotometer. Transistor characteristics of the NWT circuits were obtained using a Keithley 4200 semiconductor characterization system. The NW lengths of given transistors between the source and drain were obtained from the FE-SEM image (Hitachi S-4800) and accounted for the angle between the nanowire and the electrode edges. Optical emission from the AMOLED arrays was imaged using an optical microscope, and the luminescence was quantified with an IL 1700 research radiometer equipped with a calibrated photodetector.

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